

Application Serial No. 10/729,694

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Reply to Office Action of August 8, 2006 CENTRAL FAX CENTER

Docket No. CU-3477

NOV 01 2006

Amendments To The Specification

Please replace the paragraph [0031] in the Specification at page 7-8 lines 23-24 and 1-4, respectively, with the following amended paragraph:

First, as shown in FIG. 3A, a polysilicon layer 102 and a hard-mask layer 110 for forming gates are sequentially stacked on a semiconductor substrate ~~[[140]]~~ **100** having a certain lower structure and gates G2 are formed by masking etching, and then insulating spacers 104 are formed at both sides of the gates G2.

Please replace the paragraph [0035] in the Specification at page 8-9 lines 20-24 and 1-2, respectively, with the following amended paragraph:

Referring to FIG. 3B, a first insulating film 180 is formed to a thickness of 500 ~ 1000 Å above the resultant substrate inclusive of the storage node plugs 160, and the first insulating film 180 has faster etching rate than that of a silicon nitride film 200 that works as a etching barrier film at the time of following wet-cleaning. In this process, a BPSG **(Borophosphosilicate glass)** film is adapted as the first insulating film 180.